SOI technology pushes the limits of CMOS for RF applications

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***Abstract* — This last decade Silicon-on-Insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency commercial applications pushing the limits of CMOS technology. Thanks to the thinning down of the silicon channel, SOI MOSFETs operate in fully depleted regime and short channel effects are under controlled. Besides the gate length downscaling, strain channel engineering is introduced to achieve cutoff frequencies larger than 300 GHz. SOI also presents the major advantage of providing high resistivity substrate capabilities, leading to substantially reduced substrate RF losses, crosstalk and non-linearity. High Resistivity (HR) SOI CMOS is commonly foreseen as the most promising technology for radio frequency integrated circuits and mixed signal applications.**

I. Introduction

Systems-on-Chip (SoC) and Systems-in-Package (SiP) are the most feasible solutions to fulfil the requirements of the new communication systems. Both solutions require a high performance technology with devices that provide complex digital functionalities and can easily achieve operating frequencies in the GHz range. Therefore, it appears that only the best submicron CMOS technologies could provide a feasible and cost-effective integration of the communication systems. Silicon-on-Insulator (SOI) MOSFET technology has demonstrated its potentialities for high frequency reaching cut-off frequencies close to 500 GHz for nMOSFETs [1] and for harsh environments (high temperature, radiations). Partially depleted (PD) SOI is now massively serving the 45-nm digital market where it is seen as a low-cost – low-power alternative to bulk Si. Fully depleted (FD) devices are also widely spread as they outperform existing semiconductor technologies for extremely low power analog applications [2]. The use of high-resistivity (HR) substrates is mandatory for the design of high performance radio frequency integrated circuits (RFIC). HR-Si cannot be introduced in the case of bulk Si MOSFETs due to latch-up problem between devices. Contrary, SOI presents the major advantage of providing high resistivity substrate capabilities since the buried oxide (BOX) isolates the thin top silicon active layer from the Si handle Si substrate, leading to substantially reduced substrate losses, crosstalk and non-linearity. Substrate resistivity values higher than 1 kΩ-cm can easily be achieved.

II. High Resistivity SOI Substrate

In 1997, UCL presented pioneering work on the RF performance of high-resistivity (HR) SOI substrate material. The great interest of HR SOI substrate to reduce RF losses as well as crosstalk in Si-based substrates was presented in [3]. It has been demonstrated in [4] that HR-Si must present an effective resistivity as high as 3 kΩ.cm to be considered low loss for RF applications. However, oxidized HR-Si substrate suffers from parasitic surface conduction (PSC) due to fixed oxide charges which attract free carriers near the Si/SiO_2 interface, thereby reducing the substrate effective resistivity (ρ_{eff}) of the wafer by more than one order of magnitude compared with the bulk nominal resistivity.

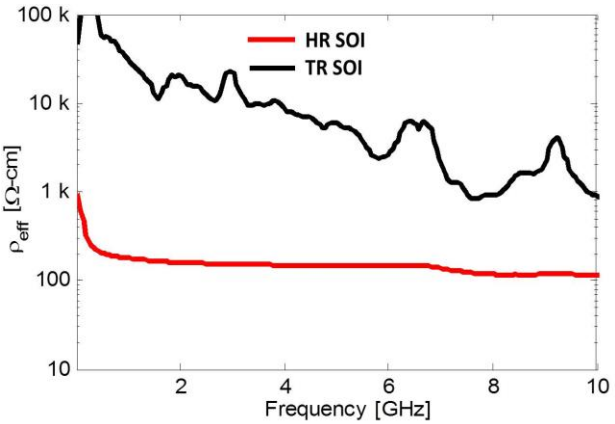

Fig. 1. Measured effective resistivity of a high-resistivity SOI substrate (HR SOI) and a trap-rich (TR SOI, i.e. eSI TR-SOI from Soitec) HR SOI substrate presenting both of them a handle Si substrate characterized by a nominal resistivity of 10 kΩ.cm.

In 2005, UCL presented the possibility of creating HR SOI substrates characterized with an effective resistivity as high as 10 kΩ.cm (Fig. 1) thanks to the silicon surface modification below the buried oxide (BOX) of a high resistivity SOI substrate. The surface modification consists in the introduction of a high density of defects called traps at the BOX / HR-Si handle substrate [5]. Those traps originate from the grain boundaries in a thin (300 nm-thick) polysilicon layer. This high-resistivity characteristic, which is conserved after a full CMOS process, translates to very low RF insertion loss (< 0.15 dB/mm at 1 GHz) along coplanar waveguide (CPW) transmission lines and purely capacitive crosstalk similarly to quartz substrate. It has been demonstrated that the presence of a trapping layer does not alter the DC or RF behavior of SOI MOS transistors [6]. Besides the insertion loss issue along interconnection lines, the generation of harmonics in Si-based substrates has been investigated [7]. UCL demonstrated that harmonics level originated from the substrate is reduced by at least 20 dB moving from standard resistivity SOI substrate (~ 10 Ω.cm) to high resistivity SOI (~ 1 kΩ.cm), and more importantly an additional drop of 40 dB is achieved with the innovative

trap-rich HR SOI (TR SOI) substrate, as illustrated in Fig. 2. This low harmonic level is comparable with insulating substrate. The improvement of the HR SOI substrate with the introduction of defects brings also clear benefits for the integration of passives, such as the quality factor of spiral inductors [8], tunable MEMS capacitors [8], as well as for the reduction of the substrate noise (crosstalk) between devices integrated on the same chip [6].

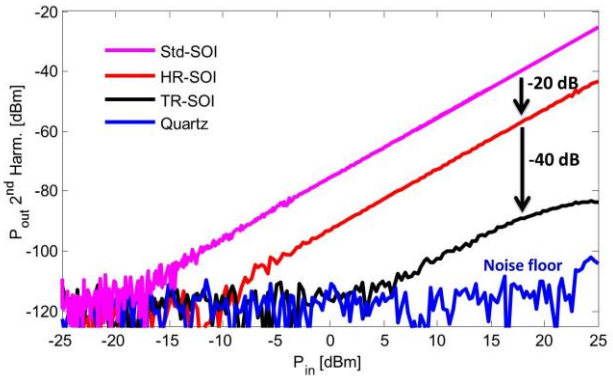

Fig. 2. Measured harmonic distortion along a CPW line lying on standard SOI (~ 10 Ω.cm) and HR based-Si substrates (~ 10 kΩ.cm) with (TR SOI, i.e. eSI TR-SOI from Soitec) and without (HR SOI) trap-rich layer.

UCL and Soitec have been working together to identify the technological opportunities to still further improve the high-frequency performance of commercially available HR-SOI substrates. Thanks to the introduction of an engineering substrate handle, Soitec has ramped up in early 2012 a new flavor of HR-SOI called eSI™, for enhanced Signal Integrity substrate with a measured effective resistivity beyond 3 kΩ.cm. Thanks to the introduction of eSI, the RF SOI substrate can really be considered as a lossless Si-based substrate. Beyond switch, eSI RF-SOI technology opens the path to further system integration in the Front End Module space as well as even more complex mixed signal System-on-Chip (SoC) [9]. As pointed out by several press releases published in 2013 and 2014 [10], the demand for the newly developed HR-SOI is booming and it is becoming the major material for high-performance RF applications. All major foundries in the field of RF applications have adopted the newly developed HR SOI substrate (Fig. 3).

III. Fully Depleted SOI MOSFET

Over the last decades silicon technology has been driven by downscaling dictated by the need of highly-integrated digital circuits. However, further reduction of device dimensions is problematic due to intrinsic physical limitations such as short channel effects (SCE), high current leakage through gate dielectrics, high series resistances, low mobility due to interface effects and high doping levels, and so on. The most common strategies to address these challenges include the introduction of new materials such as germanium, high-k gate dielectrics and metal gates, low-k for the backend dielectrics, SOI technology, strain engineering and alternative device architectures (multiple gate, i.e. FinFET, tunnel FET, etc.).

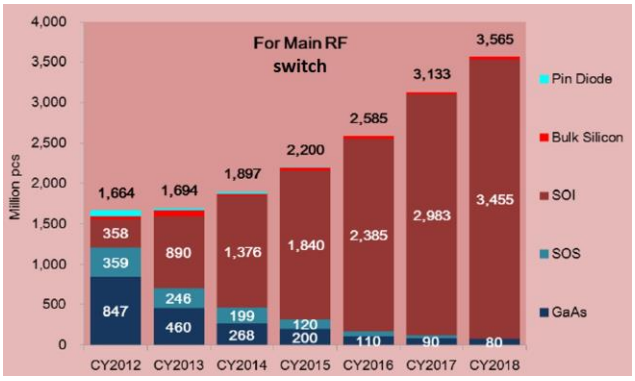

Fig. 3. Rapid adoption of the RF SOI technology by all the foundries for the integrated RF switches [11].

Fully depleted electronic regime is a promising approach to continue scaling of MOSFETs. Scaling the thickness of the silicon body is proposed in the case of FinFET and ultra-thin body and BOX (UTBB) technologies in order to control short channel effects [12, 13]. Thin silicon body of UTBB improves the electrostatic integrity, reduces the leakage current and allows the channel to be undoped. With undoped channel, higher drive current and steeper subthreshold slope are attained. Moreover significant improvement of variability control is achieved owing to the elimination of random dopant fluctuation. Thin BOX coupled with ground plane (GP) allows for the suppression of fringing electric fields through the BOX and substrate thus improving front-gate-to-channel controllability and reducing drain-induced-barrier-lowering (DIBL). Thin BOX device also becomes more suitable for implementing back-gate biasing schemes used for tuning device characteristics.

UTBB, called also 28 FD-SOI, were fabricated at ST-Microelectronics. They present a BOX, a Si body and an equivalent gate oxide thicknesses of 25 nm, 7 nm and 1.3 nm, respectively. The channel is strained and rotated by 45° from the (100) plane. The ground-plane implantation introduced under the BOX is well-type. The gate lengths of the measured devices range from 26 nm to 1 µm. More details about the process can be found in [14].

Fig. 4 shows the f_T and f_{max} variations with the channel length L_g. Both f_T and f_{max} increase with L_g scaling down but f_T follows a $1/L_g$ trend (and an even weaker one in shortest devices) i.e. attenuated comparing with ideally predicted $1/L_g^2$. This is due to carrier velocity saturation, parasitic source and drain resistances R_s, R_d and extrinsic total gate capacitance C_{gge}. It is important to point out that in case of devices shorter than 90 nm, f_{max} becomes smaller than f_T.

This is due to the increase of gate resistance R_g with L_g reduction.

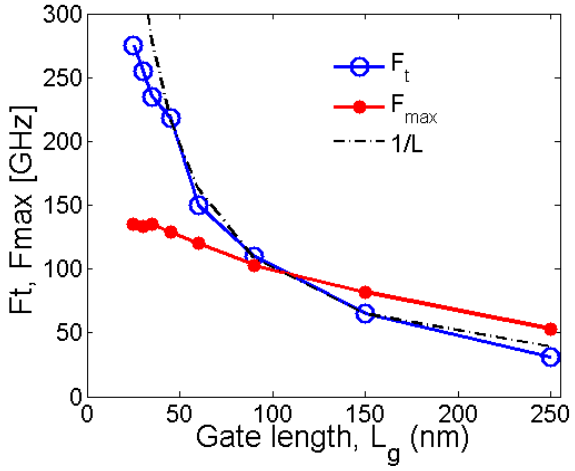

Fig. 4. f_T and f_{max} versus gate lengths (L_g) for UTBB with a channel width W_f = 2 µm and 10 gate fingers (N_f).

The benchmarking of f_T and g_m for the UTBB and other state-of-the art technologies has been presented in [15]. This study showed the direct correlation between $g_{m\text{-}max}$ and f_T. Besides the mobility boosters, an efficient improvement is achievable by optimization of process and architecture targeting reduction of parasitic series resistances and capacitances.

IV. Conclusion

Beyond its demonstrated market adoption on RF Front End Module, RF-SOI is close to be in 100% of the worldwide smartphone. In parallel, digital fully depleted SOI (FD-SOI) is also being adopted by bringing the best cost-performance trade-off at 28 nm and beyond for mobile digital devices such as application processors. It offers up to 10x lower consumption compared with standard bulk CMOS thanks to its capability to operate at much lower supply voltage and lower biasing current for equivalent processing performance. Combining advanced CMOS process with optimized SOI substrate will enable RF and digital integration for advanced SoC integration. SOI is then very well positioned to serve future 5G standards and IoT applications such as wearables that will respectively run on higher bands than today's 4G and will require drastic power consumption reduction.

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